

S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kenneth J. Janik et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	884.002US6
Title:	NON-STALLING CIRCULAR COUNTERFLOW PIPELINE PROCESSOR WITH REORDER BUFFER		
Assignee:	Intel Corporation	Customer No:	21186

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicants' prior U.S. application, Serial No. 10/391,241, filed on March 18, 2003, which is relied upon for an earlier filing date under 35 U.S.C. §120.

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Serial No :Unknown

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Title: NON-STALLING CIRCULAR COUNTERFLOW PIPELINE PROCESSOR WITH REORDER BUFFER

Assignee: Intel Corporation

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Dkt: 884.002US6 (INTEL)

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

KENNETH J. JANIK ET AL.

By their Representatives,

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"Express Mail" mailing label number: EV 298565605 US

Date of Deposit: December 9, 2003

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	Even Date Herewith
First Named Inventor	Janik, Kenneth
Group Art Unit	Unknown
Examiner Name	Donaghue, Larry

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US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,658,355	04/01/1987	Hatakeyama, et al.	712	4	
	US-5,363,495	11/08/1994	Fry, R. E., et al.	395	375	08/26/1991
	US-5,428,807	06/01/1995	McKeen, et al.	712	216	
	US-5,497,499	03/05/1996	Garg, S., et al.	395	800	03/29/1994
	US-5,572,690	11/05/1996	Molnar, C. E., et al.	395	376	06/06/1995
	US-5,600,848	02/01/1997	Sproull, et al.	712	42	
	US-5,682,493	10/01/1997	Yung, et al.	712	217	
	US-5,699,460	12/01/1997	Kopet, et al.	382	307	
	US-5,704,054	12/01/1997	Bhattacharya	712	212	
	US-5,748,936	05/01/1998	Karp, et al.	712	218	
	US-5,758,139	05/01/1998	Sutherland, et al.	713	600	
	US-5,805,838	09/01/1998	Sutherland, et al.	710	112	
	US-5,838,939	11/01/1998	Sutherland	712	200	
	US-5,913,059	06/15/1999	Torii, S.	395	674	07/25/1997
	US-5,943,491	08/01/1999	Sutherland, et al.	709	400	
	US-5,944,816	08/31/1999	Dutton, D. J., et al.	712	215	05/17/1996
	US-5,974,524	10/01/1999	Cheong, et al.	712	23	
	US-5,987,588	11/16/1999	Popescu, V., et al.	712	23	08/28/1998
	US-6,065,109	05/16/2000	Coates, W. S.	712	201	02/05/1997
	US-6,085,316	07/01/2000	Sutherland, et al.	712	245	
	US-6,185,668	02/01/2001	Arya	712	23	
	US-6,205,538	03/01/2001	Yung	712	201	
	US-6,381,692	04/01/2002	Martin, et al.	712	244	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BHANDARKAR, D. , et al., "Performance Characterization of the Pentium Pro Processor", <u>Proceedings of the Third International Symposium on High-Performance Computer Architecture</u> , San Antonio, TX, (Feb. 1-5, 1997) ,pp. 288-297	
		BURGER, D. , "The SimpleScalar Tool Set, Version 2.0", <u>University of Wisconsin-Madison Computer Sciences Department Technical Report #1342</u> , (June 1997), pp. 1-21	
		CARLSON, R. , et al., "VRP Simulator", <u>http://www.ece.orst.edu/~sllu/cfpp/vrpsim/docs/vrpsim.html</u> , (April 1996), 12 p.	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

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STATEMENT BY APPLICANT**

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Applicant Number	Unknown
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First Named Inventor	Janik, Kenneth
Group Art Unit	Unknown
Examiner Name	Donaghue, Larry

Sheet 2 of 3

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		CHILDERS, B. R., et al., "A Design Environment for Counterflow Pipeline Synthesis", <u>ACM Sigplan Workshop Proceedings on Languages, Compilers, and Tools for Embedded Systems</u> , Montreal, Canada, (June 19-20, 1998), pp. 223-234	
		CHILDERS, B. R., et al., "Application-Specific Pipelines for Exploiting Instruction-Level Parallelism", <u>University of Virginia Computer Science Technical Report No. CS-98-14</u> , (May 1, 1998), 10 p.	
		CHILDERS, B. R., et al., "Automatic Counterflow Pipeline Synthesis", <u>University of Virginia Computer Science Technical Report No. CS-98-01</u> , (Jan. 1998), 6 p.	
		CHILDERS, B. R., et al., "Synthesis of Application-Specific Counterflow Pipelines", <u>Department of Computer Science Slides of the Workshop on the Interaction between Compilers and Computer Architecture</u> , San Jose, CA, (Feb. 4, 1996), 5 p.	
		JANIK, KENNETH J., et al., "Advances of the Counterflow Pipeline Microarchitecture", <u>IEEE Computer Soc. Press - Proceedings of the Third International Symposium on High-Performance Computer Architecture</u> , (1997), 7 p.	
		JANIK, K. J., et al., "Synchronous Implementation of a Counterflow Pipeline Processor", <u>Proceedings of the 1996 International Symposium on Circuits and Systems</u> , 4, (May 12-15, 1996), 6 p.	
		JONES, M. D., "A New Approach to Microprocessors", http://lal.cs.byu.edu/people/jones/latex/sproull.html/sproull.html.html , (1994), pp. 1-17	
		JONES, MICHAEL D., "Future Computer Plumbing", <u>Insight</u> , 10 (1), (1994), pp. 50-61	
		JOSEPHS, M. B., et al., "Formal design of an asynchronous DSP counterflow pipeline: a case study in Handshake Algebra", <u>Proceedings of the International Symposium on Advanced Research in Asynchronous Circuits and Systems</u> , Salt Lake City, Utah, (Nov. 3-5, 1994), pp. 206-215	
		KORVER, "Asynchronous implementation of the SCPP-A counterflow pipelined processor", pp. 287-294	
		LO, J. L., et al., "Converting Thread-Level Parallelism to Instruction-Level Parallelism via Simultaneous Multithreading", <u>ACM Transactions on Computer Systems</u> , 15 (3), (Aug. 1997), pp. 322-354	
		MILLER, et al., "Non-Stalling Counterflow Architecture", (Feb., 1998), 334-341	
		SMITH, J. E., et al., "The Microarchitecture of Superscalar Processors", <u>Proceedings of the IEEE</u> , 83 (12), (Dec. 1995), pp. 1609-1624	
		SPROULL, ROBERT F., et al., "The Counterflow Pipeline Processor Architecture", <u>IEEE Design & Test of Computers</u> , Vol. 11, No. 5, (Fall 1994), pp. 48-59	

EXAMINER**DATE CONSIDERED**

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Group Art Unit	Unknown
Examiner Name	Donaghue, Larry

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Attorney Docket No: 884.002US6

		WERNER, "Asynchronous Processor Survey", <u>IEEE</u> , (Nov. 1997), 67-76	
		WERNER, et al., "Counterflow Pipeline Based Dynamic Instruction Scheduling", <u>IEEE</u> , 69-79	
		YAKOVLEV, A. , "Designing Control Logic for Counterflow Pipeline Processor Using Petri Nets", <u>University of Newcastle upon Tyne Technical Report No. 522</u> , (May 3, 1995), pp. 1-24	

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